IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re divisional patent application of 09/690,875 filed on October 18, 2000

Cohen et al.

Serial No.: Not Yet Assigned — Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith — Examiner: Unknown

For: DOUBLE-GATE FET WITH PLANARIZED SURFACES AND SELF ALIGNED SILICIDES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. All of these references were either cited or submitted in parent Application No. 09/690,875 and thus copies of these references are not provided in accordance with 37 C.F.R. §1.98(d).

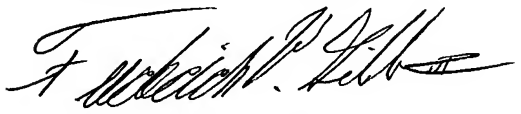
This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

YOR920000173US2

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0510.

Respectfully submitted,



Frederick W. Gibb, III
Registration No. 37,629

Date: 7/29/03

McGinn & Gibb, PLLC
2568-A Riva Road, Suite 304
Annapolis, Maryland 21401
(301) 261-8071
Customer No. 28211

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
YOR920000173US2	Not Yet Assigned
Cohen et al.	
FILING: Concurrently Herewith	GROUP: Unknown

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		5,102,819	04/07/1992	Matsushita et al.			
		5,120,666	06/09/1992	Gotou			
		5,166,084	11/24/1992	Pfiester			
		5,273,921	12/28/1993	Neudeck et al.			
		5,371,401	12/06/1994	Kurita			
		5,461,250	10/24/1995	Burghartz et al.			
		5,497,019	05/05/1996	Mayer et al.			
		5,646,058	07/08/1997	Taur et al.			
		5,708,286	01/13/1998	Uesugi et al.			
		5,773,331	06/30/1998	Solomon et al.			
		5,923,963	07/13/1999	Yamanaka			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		JP-05-226655	09/1993	Japan				✓

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			"0.18-um Fully-Depleted Silicon-on-Insulator MOSFET's", Min Cao, Ted Kamins, Paul Vande Voorde, Carlos Diaz, and Wayne Greene, IEEE Electron Device Letters, Vol. 18, No. 6, June 1997, pp.251-252
			"Super Self-Aligned Double-Gate (SSDG) MOSFET's Utilizing Oxidation Rate Difference and Selective Epitaxy", Jong-Ho Lee, Gianni Taraschi, Andy Wei, Tom A. Langdo, Eugene A. Fitzgerald, and Dimitri A. Antoniadis, Microsystems Technology Laboratories, Massachusette Institute of Technology, Cambridge, MA, IEEE, 1999, pp71-74

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY DOCKET NO.	SERIAL NO.
YOR920000173US2	Not Yet Assigned
Cohen et al.	
FILING: Concurrently Herewith	GROUP: Unknown

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,143,582	11/07/2000	Vu et al.			
		6,346,446	02/12/2002	Ritenour			
		6,365,465	04/02/2002	Chan et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

			"Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel", Hon-Sum Philip Wong, Kevin K. Chan, and Yuan Taur, IBM Thomas J. Watson Research Center, Yorktown Heights, NY, IEEE 1997, pp. 427-430
			"New Planar Self-Aligned Double-Gate Fully-Depleted P-MOSFET's Using Epitaxial Lateral Overgrowth (ELO) and Selectively Grown Source/Drain (S/D), Taichi Su, John P. Denton, and Gerold W. Neudeck, IEEE School of Electrical and Computer Engineering, Perdue University, West Lafayette, IN, IEEE, 2000, pp. 110-111

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference consid red, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.